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| 10/525,999 | 11/28/2005 | Stefan Horeth | 10808/193 | 6219 |

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| EXAMINER | |
|---|---|
| PARIHAR, SUCHIN | |
| ART UNIT | PAPER NUMBER |
| 2825 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/525,999 | HORETH ET AL. | |
| | Examiner | Art Unit | |
| | SUCHIN PARIHAR | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *6/17/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This FINAL office action is in response to application 10/525,999, amendment filed on 6/17/2008. Claims 1, 12, 13 and 15-17 are currently amended. Claim 8 is cancelled. Claims 1-7 and 9-17 are currently pending in this application.

2. Applicant's arguments filed on 6/17/2008 have been fully considered but they are not persuasive. The applicable rejections from the previous office action are incorporated herein.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. **Claims 1, 4-6, 9-12 and 14-17 are rejected under 35 U.S.C. 102(a)** as being anticipated by Jain et al. (US 6,301,687).

5. With respect to claim 1 Jain teaches:

(a) determining (determining, i.e. verifying, Col 1, lines 45-60) for specific circuit structures (circuit structure, see Abstract) described by the reference description (design specification, Col 1, lines 45-55) of the digital circuit (digital circuit designs, see Abstract), for which different implementation alternatives (different implementations of the same design, Col 1, lines 45-55) are known, in each case that an implementation alternative that has the greatest degree of structural equivalence (checking equivalence by verifying the using different implementations, Col 1, lines 45-55) with the digital

circuit to be verified (original specification, Col 1, lines 45-55), is determined, whereby the different implementation alternatives are simulated respectively (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) in combination with the reference description and compared (different implementations of the same design are compared to the circuit design, Col 1, lines 45-55) with a corresponding simulation of the digital circuit (extensive simulation to produce the "golden specification", Col 1, lines 30-55), in order to determine as the implementation alternative with the greatest degree of structural equivalence (checking equivalence by verifying using different implementations, Col 1, lines 45-55) with the digital circuit, the implementation alternative, which in this case for several simulation patterns (first implementation .... it becomes the specification for the next implementation comparison, Col 1, lines 50-65) has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit,

(b) replacing (it becomes [i.e. replaces] the specification for the next implementation, Col 1, lines 45-60) in the reference description of the digital circuit, the description of the individual circuit structures is replaced (once the implementation is verified successfully, it becomes the specification for the next implementation comparison, Col 1, lines 45-55) by the implementation alternative determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence (different implementations of the same design are compared to check their equivalence,

Col 1, lines 45-60, results in the implementation with the greatest degree of equivalence being chosen or pointed out) in each case, and

(c) executing (verification executed, Col 3, lines 15-25) the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

6. With respect to claim 14, Jain teaches:

with first memory (computer memory required for operation, Col 3, lines 25-50) means for storing (simulation results stored, Col 8, lines 60-65) a description of a digital circuit to be verified,

with second memory means (computer memory required for operation, Col 3, lines 25-50) for storing a reference description of the digital circuit (storing gate-level information, Col 8, lines 35-45), and

with verification means, which are set up in such a manner that they-the verification means compare the description of the digital circuit to be verified with the reference description (checking equivalence by verifying the using different implementations, Col 1, lines 45-55), in order through an equivalence test to recognize errors in the digital circuit, wherein

third memory means (computer memory required for operation, Col 3, lines 25-50) are provided for storing different predefined implementation alternatives (simulation results stored, Col 8, lines 60-65) for specific circuit structures of the digital circuit, whereby the verification means are set up in such a manner that, for the specific circuit

structures in each case, the verification means determine an implementation alternative (different implementations of the same design, Col 1, lines 45-55) that has the greatest degree of structural equivalence with the digital circuit to be verified (checking equivalence by verifying the using different implementations, Col 1, lines 45-55),

the verification means are set up in such a manner that, for determining the implementation alternative with the greatest degree of structural equivalence with the digital circuit in each case, the verification means simulate (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) the different implementation alternatives respectively in combination with the reference description and compare the simulations with a corresponding simulation of the digital circuit (verifying the first implementation against the original specification through extensive simulation, Col 1, lines 30-60), to determine the implementation alternative with the greatest degree of structural equivalence (see "golden specification, i.e. using the implementation with the highest degree of structural equivalence, Col 1, lines 30-50) with the digital circuit, which for simulation patterns has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit, and

the verification means are set up in such a manner that the verification means they insert (once the implementation is verified, it becomes [i.e. it is inserted as] the specification for the next implementation equivalence test, Col 1, lines 45-55) the previously determined implementation alternatives with the greatest degree of structural equivalence respectively in the reference description of the digital circuit for the

individual specific circuit structures and compare the description of the digital circuit to be verified with the reference description thus changed (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55) for executing the equivalence test (once the implementation is verified, it becomes [i.e. it is inserted as] the specification for the next implementation equivalence test, Col 1, lines 45-55).

7. With respect to claim 15, Jain teaches:

wherein a digital circuit to be verified (first implementation to be verified, Col 1, lines 45-60) is compared with a reference description (original specification [i.e. reference description], Col 1, lines 45-60) of the digital circuit, in order, to recognize errors (to catch design errors early in the design cycle, Col 1, lines 45-50) in the digital circuit using an equivalence test (verifying the equivalence of two boolean networks, Col 2, lines 10-20), the method comprising:

(a) determining (determining, i.e. verifying, Col 1, lines 45-60) for specific circuit structures (circuit structure, see Abstract) described by the reference description (design specification, Col 1, lines 45-55) of the digital circuit (digital circuit designs, see Abstract), for which different implementation alternatives (different implementations of the same design, Col 1, lines 45-55) are known, in each case that an implementation alternative that has the greatest degree of structural equivalence (checking equivalence by verifying the using different implementations, Col 1, lines 45-55) with the digital circuit to be verified (original specification, Col 1, lines 45-55), is determined, whereby the different implementation alternatives are simulated respectively (pattern simulations

used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) in combination with the reference description and compared (different implementations of the same design are compared to the circuit design, Col 1, lines 45-55) with a corresponding simulation of the digital circuit (extensive simulation to produce the "golden specification", Col 1, lines 30-55), in order to determine as the implementation alternative with the greatest degree of structural equivalence (checking equivalence by verifying using different implementations, Col 1, lines 45-55) with the digital circuit, the implementation alternative, which in this case for several simulation patterns (first implementation …. it becomes the specification for the next implementation comparison, Col 1, lines 50-65) has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit,

(b) replacing (it becomes [i.e. replaces] the specification for the next implementation, Col 1, lines 45-60) in the reference description of the digital circuit, the description of the individual circuit structures is replaced (once the implementation is verified successfully, it becomes the specification for the next implementation comparison, Col 1, lines 45-55) by the implementation alternative determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence (different implementations of the same design are compared to check their equivalence, Col 1, lines 45-60, results in the implementation with the greatest degree of equivalence being chosen or pointed out) in each case, and

(c) executing (verification executed, Col 3, lines 15-25) the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

8. With respect to claims 16 and 17, Jain teaches:

wherein a digital circuit to be verified (first implementation to be verified, Col 1, lines 45-60) is compared with a reference description (original specification [i.e. reference description], Col 1, lines 45-60) of the digital circuit, in order, to recognize errors (to catch design errors early in the design cycle, Col 1, lines 45-50) in the digital circuit using an equivalence test (verifying the equivalence of two boolean networks, Col 2, lines 10-20), the method comprising:

(a) determining (determining, i.e. verifying, Col 1, lines 45-60) for specific circuit structures (circuit structure, see Abstract) described by the reference description (design specification, Col 1, lines 45-55) of the digital circuit (digital circuit designs, see Abstract), for which different implementation alternatives (different implementations of the same design, Col 1, lines 45-55) are known, in each case that an implementation alternative that has the greatest degree of structural equivalence (checking equivalence by verifying the using different implementations, Col 1, lines 45-55) with the digital circuit to be verified (original specification, Col 1, lines 45-55), is determined, whereby the different implementation alternatives are simulated respectively (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) in combination with the reference description and compared (different implementations of

the same design are compared to the circuit design, Col 1, lines 45-55) with a corresponding simulation of the digital circuit (extensive simulation to produce the "golden specification", Col 1, lines 30-55), in order to determine as the implementation alternative with the greatest degree of structural equivalence (checking equivalence by verifying using different implementations, Col 1, lines 45-55) with the digital circuit, the implementation alternative, which in this case for several simulation patterns (first implementation .... it becomes the specification for the next implementation comparison, Col 1, lines 50-65) has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit,

(b) replacing (it becomes [i.e. replaces] the specification for the next implementation, Col 1, lines 45-60) in the reference description of the digital circuit, the description of the individual circuit structures is replaced (once the implementation is verified successfully, it becomes the specification for the next implementation comparison, Col 1, lines 45-55) by the implementation alternative determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence (different implementations of the same design are compared to check their equivalence, Col 1, lines 45-60, results in the implementation with the greatest degree of equivalence being chosen or pointed out) in each case, and

(c) executing (verification executed, Col 3, lines 15-25) the equivalence test is executed by comparing the digital circuit with the reference description changed in

accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

9. With respect to claim 4, Jain teaches:

wherein the process is executed computer-aided (computer-aided design, see Col 1, lines 10-15).

10. With respect to claim 5, Jain teaches:

wherein the reference description is selected from the group comprising RTL, VHDL and verilog descriptions (the original design is represented as an RTL design, Col 1, lines 45-55).

11. With respect to claim 6, Jain teaches:

the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

12. With respect to claim 9, Jain teaches:

wherein for each circuit structure, the different implementation alternatives are simulated at the same time and compared with the simulation of the digital circuit (extensive simulation and comparing different implementations of the same design to check for equivalence, i.e. verification, Col 1, lines 45-55).

13. With respect to claim 10, Jain teaches:

wherein the different implementation alternatives for each circuit structure are simulated at the same time by inputs (test vectors that represent all possible inputs to

the system, Col 1, lines 1-30) of the implementation alternatives being connected with one another and corresponding outputs (outputs of these test vectors are analyzed, Col 1, lines 1-30) of the implementation alternatives being led to a common output (common output, see Figure 13A) to maintain the circuit function of the individual implementation alternatives.

14. With respect to claim 11, Jain teaches:

wherein the outputs of different implementation alternatives are connected by a logic OR link to the common output (see Figure 13A).

15. With respect to claim 12, Jain teaches:

wherein for each implementation alternative in step (a). the degree of equivalence with the simulation of the digital circuit is obtained by the number of the values output for the individual simulation patterns of the reference description with the respective implementation alternative, the alternative values identically output, which are identical to the values output by the digital circuit for the corresponding simulation patterns, being determined for the several simulation patterns for each implementation alternative and being used as degree of equivalence for the corresponding implementation alternative (outputs are analyzed to try to verify their equivalence, Col 14, lines 40-45).

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claims 2, 3 and 7 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Jain et al. (6,301,687) in view of Higgins et al. (6,993,730).

18. With respect to claim 2, Jain fails to teach:

wherein the specific circuit structures for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures.

However, Higgins teaches:

wherein the specific circuit structures for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures (equivalencies between two multiplier circuits, Col 12, lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Higgins into the invention of Jain for at least the following reason: Higgins improves the invention of Jain by providing a method that can determine equivalence between two circuit models much quicker than previously attainable in the prior art (see Abstract).

19. With respect to claim 3, Higgins teaches:

wherein he specific circuit structures, for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures for realizing integral multiplication function (equivalencies between two multiplier circuits, Col 12, lines 25-35).

20. With respect to claim 7, Jain fails to teach:

wherein the pre-defined implementation alternatives for the specific circuit structures comprise varying architectures of the specific circuit structures aided by a synthesis device available for the design of the digital circuit.

However, Higgins teaches more than one architecture for the specific circuit structures that are multipliers (equivalencies between two multiplier circuits, Col 12, lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Higgins into the invention of Jain for at least the following reason: Higgins improves the invention of Jain by providing a method that can determine equivalence between two circuit models much quicker than previously attainable in the prior art (see Abstract).

***Response to Arguments***

21. Applicant's arguments filed on 6/17/2008 have been fully considered but they are not persuasive. Examiner's response to Applicant's remarks follow below:

22. Applicant asserts that the term "implementation alternative" of claim 1 is different than the reference's [i.e. Jain et al.] "different implementations of the same design" in Col 1, lines 45-55 of Jain. Applicant goes on to explain that "implementation alternative", according to the claimed invention, describes one of a plurality of possible alternatives to implement a specific circuit "unction in different alternative ways as described on page 2, line 14 to 32 of the present application. Examiner disagrees with this assertion.

23. First, Examiner points out that: limitations from the specification do no read into the claims. Therefore, the claims do no rely upon the above description of “implementation alternative” unless the claims recite such language. Additionally, page 2 lines 14-32 of Applicant's specification point out that "implementation alternatives" have possibly only a few internal equivalences. Jain analogously points out "internal equivalences" of two different networks in Col 6, lines 25-45. Second, when Applicant asserts on page 11 of the remarks that “a plurality of possible alternatives to implement a specific circuit function”, it is in fact the same circuit function being implemented in each alternative. Therefore, Jain teaches "implementation alternative" (different implementations [i.e. alternatives] of the same design [i.e. specific circuit functions(s)]. See Jain, Col 1, lines 45-60).

24. Applicant asserts that Jain fails to disclose “an implementation alternative with the greatest degree of structural equivalence”. Examiner disagrees with this assertion.

25. Examiner points out that an implementation with the greatest degree of structural equivalence is determined effectively as a result of Col 1, lines 45-60 of Jain. In Col 1, lines 45-60 of Jain, a first implementation of a circuit is compared to an original specification [i.e. reference description] and if that first implementation is equivalent, then that first implementation replaces the original specification, and then the new original specification [i.e. the first implementation] is compared for equivalence to the second implementation, and so on until the original specification is replaced with an implementation that is of the highest degree of structural equivalence. Additionally, Applicant’s specification describes equivalence using terms such as "points of

equivalence" on page 14 line 20 and "internal equivalence" on page 2 lines 30-32. Jain also describes equivalence with such terms as "equivalent points" (Col 2, lines 40-50) and "internal equivalences" (Col 6, lines 25-45). Therefore, both Jain and Applicant's invention use the term equivalence in the same manner.

26. Applicant asserts that Jain fails to teach or suggest replacing specific structures or parts of the complete circuit. Examiner disagrees with this assertion.

27. Examiner points out that, per claim 1, it is recited "replacing in the reference description of the digital circuit, the description of the individual circuit structures by the implementation alternative determined for the respective circuit structure". Examiner has interpreted said recitation as the entirety of the description being replaced by individual structures one at a time until the entire description is replaced. Examiner does not interpret said language to mean that only a part or few parts are replaced only. Examiner suggests amending the language to clarify the meaning if it is intended to mean that only a part or few parts are replaced and not the entire description. However as it is recited currently, Jain teaches: replacing in the reference description of the digital circuit, the description of the individual circuit structures by the implementation alternative determined for the respective circuit structure (once an implementation has been verified, it becomes the specification for the next implementation).

28. Applicant asserts that Jain fails to teach: performing an equivalence test of a circuit description to an original specification or a modified specification of the digital circuit. Examiner disagrees with this assertion.

29. Examiner points out that Col 1, lines 45-60 of Jain describes a equivalence test process where a circuit implementation is compared to its original specification to determine whether the implementation is equivalent. If it is, then the original specification gets replaced by the implementation and becomes the new original specification. Therefore, Col 1 lines 45-60 of Jain teaches such an equivalence test.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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